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High-Performance Low-Cost Back-Channel-Etch Amorphous Gallium–Indium–Zinc Oxide Thin-Film Transistors by Curing and Passivation of the Damaged Back Channel

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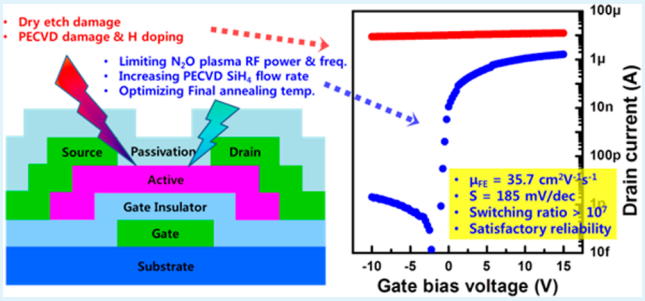
Supporting Information

ABSTRACT: High-performance, low-cost amorphous gallium–indium–zinc oxide (a-GIZO) thin-film-transistor (TFT) technology is required for the next generation of active-matrix organic light-emitting diodes. A back-channel-etch structure is the most appropriate device structure for high-performance, low-cost a-GIZO TFT technology. However, channel damage due to source/drain etching and passivation-layer deposition has been a critical issue. To solve this problem, the present work focuses on overall back-channel processes, such as back-channel N_2O plasma treatment, SiO_x passivation deposition, and final thermal annealing. This work has revealed the dependence of a-GIZO TFT characteristics on the N_2O plasma radio-frequency (RF) power and frequency, the SiH_4 flow rate in the SiO_x deposition process, and the final annealing temperature. On the basis of these results, a high-performance a-GIZO TFT with a field-effect mobility of 35.7 $cm^2\ V^{-1}\ s^{-1}$, a subthreshold swing of 185 mV dec^{-1}, a switching ratio exceeding 10^7, and a satisfactory reliability was successfully fabricated. The technology developed in this work can be realized using the existing facilities of active-matrix liquid-crystal display industries.



KEYWORDS: *annealing, back-channel etch, field-effect transistor, gallium–indium–zinc oxide, N_2O plasma, passivation*

INTRODUCTION

Amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) are expected to become a major TFT technology[1−3] because of their high performance and low production costs compared to other TFT technologies. The high field-effect mobility (μ_{FE}) of AOS TFTs makes it possible to substitute these transistors for polycrystalline silicon TFTs (poly-Si TFTs) as switching devices for active-matrix organic light-emitting diodes (AMOLEDs). Generally speaking, a μ_{FE} value higher than 10 $cm^2\ V^{-1}\ s^{-1}$ can easily be obtained for AOS TFTs,[4−6] and such a value is high enough for the pixel-driving circuits of AMOLEDs. Additionally, the production costs of AOS TFTs can be kept as low as those of amorphous silicon (a-Si) TFTs because their fabrication processes are similar. Therefore, both the high performance of poly-Si TFTs and the low production costs of a-Si TFTs can be simultaneously realized by AOS TFTs. Moreover, AOS TFTs can be used for novel devices such as transparent displays and smart windows, thanks to the transparency of AOS.[7−9]

Among the various AOS TFTs, amorphous gallium–indium–zinc oxide (a-GIZO) TFTs have received the most attention[1,3,5,10,11] because the process window for obtaining a-GIZO TFTs with suitable switching performance and stability is wider than those of other AOS TFTs. Numerous reports have been published about high-performance, stable a-GIZO TFTs,[11−13] and commercialization of a-GIZO TFTs has recently been undertaken by active-matrix flat-panel display (AMFPD) industries. In the AMFPD market, product pricing is one of the most essential factors. Hence, the lower the production costs are, the better the market penetration of a-GIZO TFTs will be. Two types of device structures are available for typical a-GIZO TFTs: etch stopper (ES)[12,14,15] and back-channel etch (BCE).[16−18] The ES structure facilitates the fabrication of high-performance, stable a-GIZO TFTs because the ES protects the back channel from damage caused by upper-layer processing.[14,19] However, the device structure of ES TFTs is more complex, and the production costs are higher than those of BCE TFTs. Therefore, it is important to develop a BCE a-GIZO TFT technology that provides a level of performance suitable for commercial AMFPDs. A source/drain dry-etch method is more appropriate than a wet-etch method for fabricating high-resolution AMFPDs, and a passivation layer is required to protect the channel layer of an a-GIZO TFT from the external environment. Hence, these procedures should be

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included in the BCE a-GIZO TFT technology. Moreover, in the BCE a-GIZO TFT fabrication process, source/drain dry etching[20,21] and passivation-layer deposition[22,23] are closely related to device performance degradation. To reduce the degradation and obtain a proper switching performance, back-channel N_2O plasma treatment has been suggested and has proven to be effective.[20,24] In addition to the performance improvement, the device stability is also improved by N_2O plasma treatment.[25] Some reports have focused on passivation layers for BCE a-GIZO TFTs.[23,26] However, to establish BCE a-GIZO TFT technology for commercial mass production, it is necessary to systematically study the upper-layer fabrication processes on the back channel. The back-channel treatment, passivation-layer deposition, and final annealing processes should be included in this kind of research because all of these steps influence the back-channel properties. To our knowledge, no papers have been published about this issue.

In this study, we investigated the effects of upper-layer fabrication processes on the device performance of BCE a-GIZO TFTs. To understand the degradation mechanism of the source/drain BCE dry-etch process, the changes in the composition and oxygen binding energy of the a-GIZO active layers were examined because these may have been altered by the source/drain dry-etch and back-channel treatment. The device characteristics of a-GIZO TFTs were then investigated according to the upper-layer process conditions. In this way, we were able to discover key factors determining the device characteristics and obtain high-performance BCE a-GIZO TFTs with high-resolution source/drain features.

EXPERIMENTAL SECTION

The device characteristics of a-GIZO TFTs were analyzed with respect to the fabrication process conditions for the upper layers of the a-GIZO active layer. A BCE structure was employed for the a-GIZO TFTs in this work. A back-channel N_2O plasma treatment was used to restore the performance of a-GIZO channel layers degraded by the source/drain dry-etch process. The effects of back-channel treatment, passivation-layer fabrication, and final annealing on the device characteristics of these TFTs were studied under various process conditions.

Figure 1 shows a cross-sectional diagram of the type of a-GIZO TFT used in this study. A BCE bottom-gate, top-contact structure,

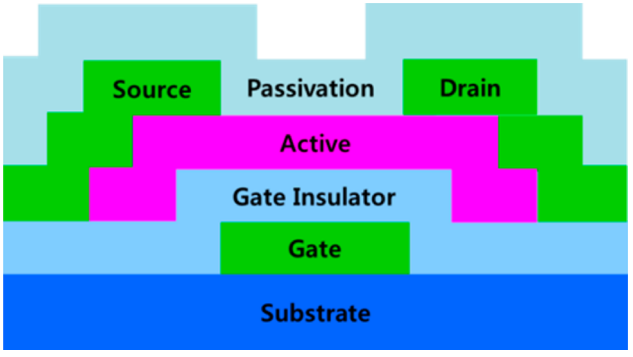

Figure 1. Cross-sectional diagram of the type of a-GIZO TFT used in this study.

which is the commonest structure for active-matrix liquid-crystal displays (AMLCDs),[27] was employed. The a-GIZO TFTs were fabricated on 6-in. thermally grown silicon dioxide/silicon substrates. After initial cleaning, a molybdenum (Mo) gate metal layer with a thickness of 150 nm was sputtered at room temperature. Gate electrode patterns were then created via a dry-etch process. An amorphous silicon oxide (SiO_x) gate insulator layer with a thickness of 100 nm was deposited on the gate electrode, using plasma-enhanced chemical vapor deposition (PECVD) at 150 °C. On the gate insulator, a GIZO active layer with a thickness of 70 nm was deposited via radio-frequency (RF) magnetron sputtering at room temperature. The GIZO target composition was a molar ratio of 1:1:1 $Ga_2O_3/In_2O_3/ZnO$, and the mixing ratio of the sputtering gas was 100:1 Ar/O_2. Next, active-island patterns were fabricated, using a wet-etch method with diluted hydrofluoric acid. A layer of Mo with a thickness of 200 nm was sputtered on the active island at room temperature. Source/drain patterns were fabricated via a dry-etch process. A SF_6/O_2 gas mixture was used for dry etching of the Mo layer; the overetch time was 60 s. Back-channel treatment with N_2O plasma was then conducted. After the back-channel treatment, a 200-nm SiO_x passivation layer was deposited without a vacuum break via PECVD at 150 °C and then patterned via a dry-etch method. After the device structure fabrication was completed, final annealing was conducted in a nitrogen atmosphere. The device structure, process sequence, and process equipment employed in the fabrication of the BCE a-GIZO TFTs were the same as those used to fabricate a-Si TFTs.

Transfer curves of the fabricated TFTs were measured using a semiconductor parameter analyzer (Agilent 4156B) in a dark shielding box. X-ray photoelectron spectroscopy (XPS) was conducted to examine the composition changes of the a-GIZO films according to the process conditions, using a PHI Quantum 2000.

RESULTS AND DISCUSSION

Device characteristics of a-GIZO TFTs were examined under various process conditions for back-channel treatment, passivation-layer deposition, and final annealing. Additionally, composition variations of the a-GIZO active layers due to source/drain dry etching and N_2O back-channel treatment were investigated. The results were analyzed to identify the optimal fabrication conditions for high-performance BCE a-GIZO TFTs.

Figure 2 shows variation of the composition and oxygen binding energy of the a-GIZO active layers depending on the source/drain dry-etching and N_2O back-channel treatment conditions. XPS measurements were conducted using a 1486.6-eV monochromatic Al Kα X-ray with a beam size of 100 μm. To enhance the bulk sensitivity of the measurements, normal emission was used as the takeoff angle. Figure 2a presents the atomic concentrations of the a-GIZO films according to the treatment conditions. These atomic concentrations were obtained from XPS analysis. Figure 2b shows deconvoluted XPS spectra of the O 1s level. The O 1s spectra were deconvoluted into three Gaussian peaks centered at ~529.8 eV (P1), ~530.8 eV (P2), and ~531.6 eV (P3), which were assigned to oxide without oxygen deficiencies, oxide with oxygen deficiencies, and hydroxide, respectively.[28−30] An as-deposited film (A) was included in the composition change analysis as a reference. A source/drain etch plasma-treated film (B) was analyzed to determine the cause of device degradation resulting from the source/drain dry-etch process. A source/drain etch plasma using an SF_6/O_2 gas mixture was applied to the a-GIZO film for 60 s, which is equal to the overetch time for the source/drain etching process. Because a-GIZO has high etch selectivity, virtually no thickness change resulted from this plasma treatment. The source/drain etch plasma decreased the oxygen concentration and increased the indium and zinc concentrations, as shown in Figure 2a. The increased metallic components may create a conductive backside layer, which, in turn, could degrade the device performance.[20,21] As shown in Figure 2b, the amount of oxide with deficiencies increased following the etch, whereas the amount of oxide without

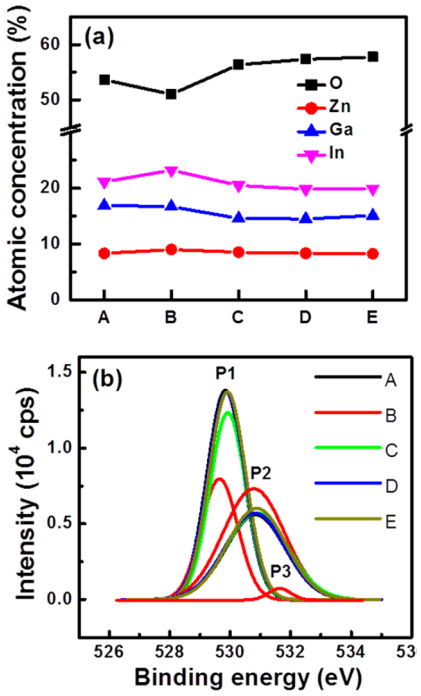

Figure 2. (a) Composition variations and (b) deconvoluted O 1s XPS spectra of the BCE a-GIZO active layers according to source/drain dry-etching and N_2O back-channel treatment conditions: as-deposited film (A); source/drain etch plasma-treated film (B); N_2O plasma films treated for 60 s (C), 120 s (D), and 180 s (E).

deficiencies decreased. In addition, a hydroxide peak appeared. The increase in the oxygen deficiencies and hydrogen incorporation may have increased the charge carrier density, which may have led to the large off-currents of the TFTs. N_2O plasma treatment was applied to the source/drain etch plasma-treated samples. The N_2O plasma treatment times of samples C−E were 60, 120, and 180 s, respectively. As the N_2O plasma treatment proceeded, the oxygen concentration increased, and the indium, zinc, and gallium concentrations decreased, as shown in Figure 2a. Figure 2b shows that the N_2O plasma treatment restored the O 1s XPS spectrum of the source/drain etch plasma-treated a-GIZO to the original form of the as-deposited a-GIZO. Peak P3 was removed by the 60 s N_2O plasma treatment. Furthermore, peak P2 was restored to the shape of as-deposited a-GIZO following the 60 s N_2O plasma treatment. The O 1s XPS spectrum was restored to that of as-deposited a-GIZO by N_2O treatment for a duration of more than 120 s. The reactive oxygen supplied by the N_2O plasma could oxidize metallic or suboxidized metal components, which could result in restoration of the O 1s XPS spectrum, an increase in the oxygen concentration, and a decrease in the metallic concentration. The decrease in the metallic concentration and oxygen deficiency may reduce the conductivity of the a-GIZO film and restore device performance.

The dependency of the device performance on the RF power of the N_2O plasma was investigated (see Figure 3). The nearly flat transfer curve of the a-GIZO TFT without N_2O plasma treatment revealed that the switching performance of the a-GIZO TFT was completely degraded by the source/drain etch plasma. An N_2O plasma treatment with mild RF power (50 W) restored this degraded performance to a high performance. The field-effect mobility (μ_{FE}), threshold voltage (V_{TH}), and subthreshold swing (S) were 35.7 $cm^2\ V^{-1}\ s^{-1}$, −3.14 V, and

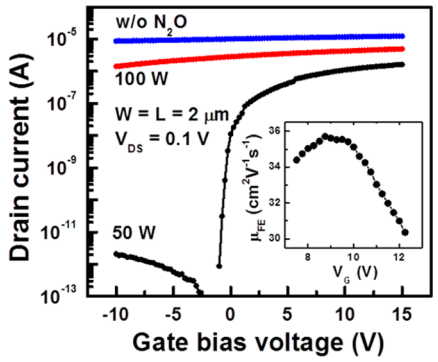

Figure 3. Drain currents of the BCE a-GIZO TFTs as functions of gate bias voltage according to the RF power of the N_2O plasma treatment. The drain bias voltage was 0.1 V, and the source was grounded. The channel width and length were both 2 μm.

185 mV dec^{-1}, respectively. A linear-mode gradual-channel approximation was used for the evaluation, and μ_{FE} was calculated via the equation

$$\mu_{FE} = \frac{\partial I_D}{\partial V_G}\frac{L}{WC_{GI}V_D} \quad (1)$$

where I_D, V_D, V_G, L, W, and C_{GI} are the drain current, drain bias voltage, gate bias voltage, channel length, channel width, and gate insulator capacitance per unit area, respectively. This result is shown as the inset of Figure 3. The value of μ_{FE} was obtained by taking the maximum of the calculated values. V_{TH} was obtained via a linear fitting of measured data to the equation

$$I_D = \frac{W}{L}C_{GI}\mu_{FE}(V_G - V_{TH})V_D \quad (2)$$

In contrast with the 50 W N_2O plasma-treated case, the a-GIZO TFT treated with high-RF-power (100 W) N_2O plasma had no switching capability. N_2O is preferable to O_2 for backside plasma treatment of BCE a-GIZO TFTs because the enthalpy of oxygen formation is considerably lower for N_2O (1.73 eV) than for O_2 (4.13 eV). This comparatively easy formation of oxygen from N_2O could reduce ion-bombardment damage during the backside treatment. Hence, the high-performance a-GIZO TFT could be fabricated using 50 W N_2O plasma treatment. However, even with N_2O gas, high-RF-power plasma treatment can induce damage and degrade the device performance, as in the case of the 100 W N_2O-plasma-treated a-GIZO TFT in Figure 3. Consequently, by adopting N_2O plasma back-channel treatment and restricting its RF power, BCE a-GIZO TFTs with a suitable switching performance can be obtained.

The dependence of the device performance on the RFs of the N_2O plasma treatment and SiO_x passivation-layer deposition was examined. Devices were fabricated using a 120 s N_2O plasma treatment and a 200 nm SiO_x passivation layer. Figure 4 shows the transfer curves of the BCE a-GIZO TFTs according to the RFs. When the RFs of the N_2O treatment and SiO_x deposition were both as high as 13.56 MHz, the switching capability was completely eliminated. When the RF of the N_2O treatment was as high as 13.56 MHz and the RF of the SiO_x deposition was as low as 350 kHz, the switching performance of the a-GIZO TFT was rather poor. However, the BCE a-GIZO TFT fabricated with an N_2O treatment RF of 350 kHz and an SiO_x deposition RF of 13.56 MHz exhibited a high switching performance. The values of μ_{FE}, V_{TH}, and S for this device were

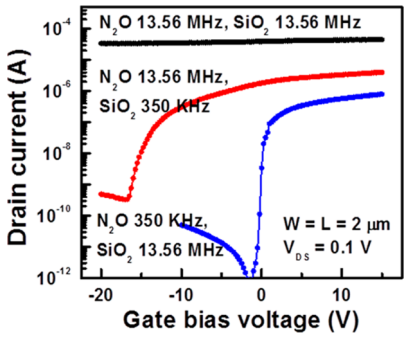

Figure 4. Drain currents of the BCE a-GIZO TFTs as functions of gate bias voltage according to the RFs of the N_2O plasma treatment and SiO_x passivation-layer deposition. The drain bias voltage was 0.1 V, and the source was grounded. The channel width and length were both 2 μm.

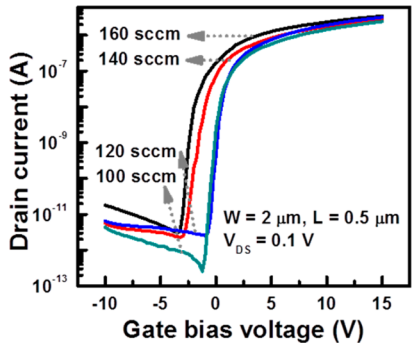

Figure 5. Drain currents of the BCE a-GIZO TFTs as functions of gate bias voltage according to the SiH_4 flow rate during the SiO_x deposition process. The drain bias voltage was 0.1 V, and the source was grounded. The channel width and length were 2 and 0.5 μm, respectively.

33.4 $cm^2\ V^{-1}\ s^{-1}$, −3.52 V, and 195 mV dec^{-1}, respectively. High-RF plasma causes large ion flux with high ion energy,[31] so the high-RF N_2O plasma treatment can induce ion bombardment damage. Hence, a-GIZO TFTs with high-RF (13.56 MHz) N_2O plasma treatment had poor switching properties. Damage caused by the intense N_2O plasma can increase the leakage current of the a-GIZO TFTs, as shown in Figure 3. In the case of 13.56 MHz N_2O and 13.56 MHz SiO_x, the high RF (13.56 MHz) of the SiO_x deposition process can result in a large energetic hydrogen flux, which may further increase the leakage current because of the role of hydrogen as a donor. In the case of 13.56 MHz N_2O and 350 kHz SiO_x, the reduced flux and energy of hydrogen in the SiO_x deposition process can result in better switching properties than those in the case of 13.56 MHz SiO_x. When a dry-etch-damaged a-GIZO layer is cured using an appropriate plasma treatment, the resistivity of the a-GIZO layer increases[21] with the incoming excess of oxygen atoms in the layer. These excess oxygen atoms can act as acceptors.[32,33] Hence, hydrogen donors could be counterbalanced by oxygen acceptors. Thus, 350 kHz N_2O plasma, as an appropriate plasma condition, could cure the dry-etch damage of a-GIZO layers as well as prevent hydrogen-related degradation. Therefore, a high-performance a-GIZO TFT, with 350 kHz N_2O and 13.56 MHz SiO_x, can be achieved.

The dependency of device characteristics on the SiH_4 flow rate during the SiO_x deposition process was examined. Hydrogen acts as a dopant in a-GIZO.[28,33,34] Hence, hydrogen incorporation into an a-GIZO layer during the SiO_x deposition process increases the conductivity of the layer. SiH_4 is the hydrogen source in the SiO_x deposition process. Figure 5 shows the transfer curves of the BCE a-GIZO TFTs according to the SiH_4 flow rate. In the SiO_x deposition process, a gas mixture of SiH_4, N_2, and N_2O was used. The flow rates of N_2 and N_2O were fixed at 240 and 1420 sccm, respectively, while the flow rate of SiH_4 was varied. The process pressure and RF were 550 mTorr and 350 kHz, respectively, for all devices shown in Figure 5. An increase in the SiH_4 flow rate caused V_{TH} to shift in the negative direction. Specifically, V_{TH} was shifted from +2.69 to −0.55 V, and μ_{FE} increased from 15.02 to 20.63 $cm^2\ V^{-1}\ s^{-1}$ as the SiH_4 flow rate was increased from 100 to 160 sccm. In addition, the off-current tended to increase with the SiH_4 flow rate. The doping effect of hydrogen may cause a higher carrier concentration at a higher SiH_4 flow rate, and a higher carrier concentration increases the mobility of a-GIZO.[35,36] This could explain the V_{TH} negative shift and the μ_{FE} increase with increasing SiH_4 flow rate. Additionally, the high carrier concentration may have been related to the high off-current that accompanied the high SiH_4 flow rate.

Next, the effects of the final annealing temperature on the device performance of BCE a-GIZO TFTs were investigated. Figure 6 presents the transfer curves of the BCE a-GIZO TFTs

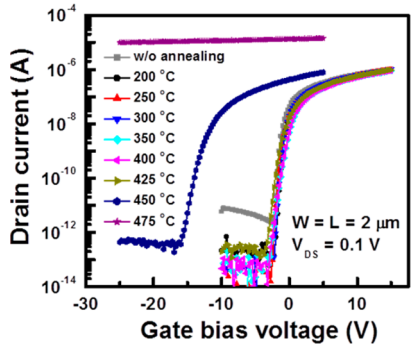

Figure 6. Drain currents of the BCE a-GIZO TFTs as functions of gate bias voltage according to the final annealing temperature. The drain bias voltage was 0.1 V, and the source was grounded. The channel width and length were both 2 μm.

according to the final annealing temperature. The annealing was conducted in an N_2 atmosphere for 1 h. At annealing temperatures of less than 425 °C, the shape of the transfer curve was virtually unchanged, except for a slightly positive V_{TH} shift as the annealing temperature increased. However, the off-current was significantly reduced by thermal annealing, compared with what was obtained without annealing. The defect-curing effect of the thermal energy may have been responsible for reducing the off-current. At temperatures above 425 °C, the final annealing significantly degraded the switching performance. The a-GIZO TFT annealed at 450 °C suffered a large negative V_{TH} shift, while 475 °C annealing completely eliminated the switching capability.

Hysteresis, negative-bias temperature stress (NBTS), and positive-bias temperature stress (PBTS) behaviors were examined (see Figure 7) using the a-IGZO TFTs developed in this work. As shown in Figure 7a, the forward- and reverse-direction transfer curves were almost identical. The drain-to-source bias voltage (V_{DS}) was 10.1 V, which is sufficiently high compared with the conventional bias voltage for AMFPD applications. Hence, the a-GIZO TFTs seem to exhibit no

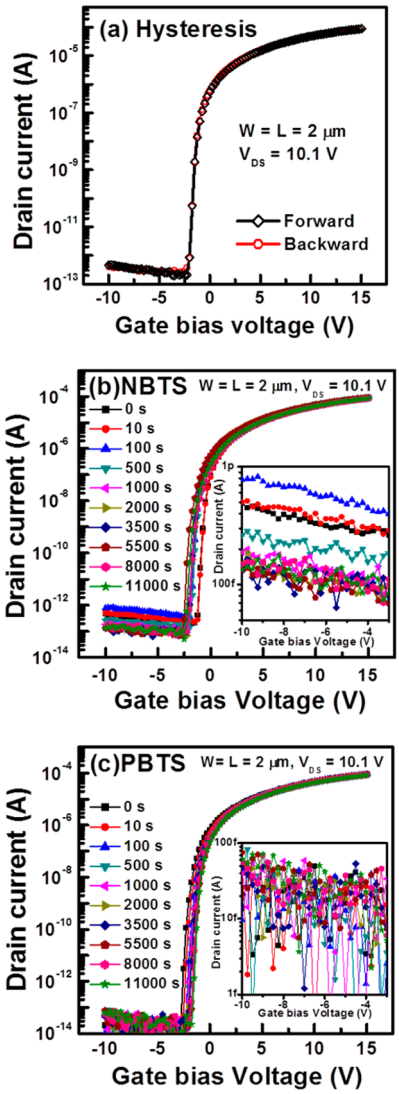

Figure 7. Transfer curves of a-GIZO TFTs obtained from reliability testing for (a) hysteresis, (b) NBTS, and (c) PBTS. The drain bias voltage was 10.1 V, and the source was grounded during measurements. The channel width and length were both 2 μm.

hysteresis properties. Parts b and c of Figure 7 present the results of NBTS and PBTS, respectively. The drain bias voltage (V_D), the source bias voltage (V_S), the gate bias voltage (V_G), and the temperature during NBTS were 10 V, 0 V, −20 V, and 60 °C, respectively, and V_D, V_S, V_G, and the temperature during PBTS were 10 V, 0 V, 20 V, and 60 °C, respectively. All transfer curves in Figure 7b,c were measured with V_{DS} at 10.1 V. For NBTS, V_{TH} shift (ΔV_{TH}) was saturated at −1 V after 100 s, and for PBTS, ΔV_{TH} was saturated at 0.75 V after 100 s. These ΔV_{TH} values were considerably smaller than those in previous reports.[37−41] To understand the leakage current properties, the off-state drain currents are shown in the insets of Figure 7b,c. For NBTS, the leakage current initially decreased with increasing stress time and finally saturated at approximately 10^{-13} A after a stress period of 1000 s. For PBTS, the leakage current was on the order of 10^{-14} A for all stress times. Therefore, the leakage current was stable in response to the bias stress.

CONCLUSIONS

The objective of our research was to establish a fabrication process for high-performance BCE a-GIZO TFTs with high-resolution features that is comparable to the process used for a-Si TFTs, in terms of both economics and practicality. For this purpose, we used a BCE bottom-gate top-contact structure, and the dependence of the device performance on the upper-layer fabrication processes was investigated.

By optimization of the upper-layer fabrication processes, including the N_2O backside plasma treatment, passivation-layer deposition, and final annealing, the damage to the channel due to the source/drain dry etch and passivation deposition could be cured and prevented. To achieve this, the RF power and frequency of the N_2O plasma should be as low as 50 W and 350 kHz. A high-SiH_4-flow-rate passivation deposition process combined with the final annealing increased μ_{FE} without an increase in the leakage current. The a-GIZO TFTs had a field-effect mobility of μ_{FE} = 35.7 cm^2 V^{-1} s^{-1}, a subthreshold slope of S = 185 mV dec^{-1}, and a switching ratio in excess of 10^7. In addition, ΔV_{TH} due to NBTS and PBTS was small compared with that of previous reports.

As the commercialization of a-GIZO TFTs proceeds, the demand for a commercial production technology for high-resolution bottom-gate top-contact BCE a-GIZO TFTs is increasing. However, this demand cannot be met using the fabrication methods of previous researches, which focus on unit processes, such as back-channel treatments[20,24,25] and exotic passivation materials.[11,41,42] In this study, we were able to meet this demand successfully by optimizing the overall processes, including the source/drain dry etch, back-channel plasma treatment, passivation deposition, and final annealing. Our devices performed better than commercially available ES a-GIZO TFTs, and the metrics are sufficient for high-quality AMFPD applications. In addition to the high performance, the short channel length (down to 0.5 μm) makes our devices appropriate for integrating high-density peripheral circuits on substrates. In addition, the device fabrication process was similar to that of conventional a-Si TFTs for AMLCDs. Hence, our fabrication process may be a core technology in the conversion of existing a-Si TFT production lines to a-GIZO TFT production lines. Therefore, we expect this work to be useful for AMFPD industries in developing competitive baseline technologies for next-generation products.

ASSOCIATED CONTENT

Supporting Information

Graphs of the variation ratios of the atomic concentrations of a-GIZO layers and O 1s XPS spectra according to backside treatment conditions, Rutherford backscattering spectrometry spectra showing indium, gallium, and zinc peaks, and scanning electron microscopy images of fabricated BCE a-GIZO TFTs. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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